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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P5771D
First Inventor or Application Identifier	Chunlin Liang
Title	Method for Making A Complementary Metal Gate Electrode Technology
Express Mail Label No.	EM014065854US

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification — Total Pages: 24 *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (*if filed*)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 CFR 113)* — Total Sheets: 4
4. Oath or Declaration — Total Pages: 3
   a. [ ] Newly executed (original copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 16 completed)* ***[Note Box 5 below]***
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

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NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO - 1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] *Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: . . . . . .

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 09 / 107,604
Prior application Information: Examiner Thompson, C. *Group/Art Unit:* 2813
For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Attorney's Docket No. 042390.P5771D
Express Mail No. EM014065845US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Gang Bai and Chunlin Liang

Serial No.

Filed:

For: *Complementary Metal Gate Electrode Technology*

Divisional Application of:
Serial No. 09/107,604
Filed: June 30, 1998

Examiner: Thompson, C.

Art Unit 2813

PRELIMINARY AMENDMENT

Box New Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In connection with the filing of the Divisional Application under Rule 1.53(b), Applicants respectfully request entry of the following amendments.

IN THE SPECIFICATION

At page 9, lines 6 and 7, please replace "diffusing" with --introducing--.

At page 9, line 14, please delete "layer".

At page 9, line 23, please delete "layer".

At page 10, lines 15 and 16, please replace "masking" with --mask--.

At page 10, line 24, please replace "masking" with --mask--.

At page 11, line 6, please replace "hard mask 135" with --mask layer 135--.

At page 11, line 9, please replace "masking" with --mask--.

At page 11, line 17, please delete "region".

At page 11, lines 2 and 21, please replace "masking" with --mask--.

At page 12, line 8, please replace "masking" with --mask--.

At page 13, line 26, please replace "P-well" with --P-type well--.

At page 14, line 1, please replace "P-well" with --P-type well--.

At page 17, line 8, please replace "of a CMOS circuit to optimum" with --to improve NMOS and PMOS--.

At page 17, line 13, please delete "layer".

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Dated: 3/2/00

William Thomas Babbitt, Reg. No. 39,591

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Docket No. 042390.P5771
Express Mail No. EM014063371US

UNITED STATES PATENT APPLICATION

FOR

COMPLEMENTARY METAL GATE ELECTRODE TECHNOLOGY

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BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates generally to the field of integrated circuit devices and more particularly to the structure of integrated circuit devices.

Background Information

The use of metal gate technology is viewed as very desirable for complementary metal oxide semiconductor (CMOS) device technology scaling below the sub 0.1 micron regime. Replacing traditional polysilicon gate electrodes with metal or metal alloy gate electrodes can significantly eliminate undesired voltage drops associated with polysilicon gate electrodes (e.g., polysilicon depletion effect) and improve device drive current performance. Metal and metal alloy gate electrodes can also reduce the parasitic resistance of the gate line and allow longer gate runners in high performance integrated circuit design for applications such as stacked gates, wordlines, buffer drivers, etc.

Conductive materials have different energies measured conventionally by their Fermi level. As an example, the Fermi level of a material determines its work function. The intrinsic Fermi level of an undoped semiconductor is at the middle of the bandgap between the conduction and valence band edges. In an N-type doped silicon, the Fermi level is closer to the conduction

band than to the valence band (e.g., about 4.15 electron-volts). In a P-type doped silicon, the Fermi level is closer to the valence band than the conduction band (e.g., about 5.2 electron-volts).

Metals or their compounds have been identified that have work functions similar to the work functions of a conventional P-type doped semiconductor substrate. Other metals or their compounds have been identified that have work functions similar to a conventional N-type doped semiconductor substrate. Examples of metals that have a work function similar to P-type doped semiconductor material, include but are not limited to, nickel (Ni), ruthenium oxide (RuO), molybdenum nitride (MoN), and tantalum nitride (TaN). Examples of metals that have a work function to N-type doped semiconductor material, include but are not limited to, ruthenium (Ru), zirconium (Zr), niobium (Nb), tantalum (Ta), molybdenum silicide (MoSi), and tantalum silicide (TaSi).

Previous proposed metal gate CMOS technology has focused on using one type of metal having a Fermi level located in the middle of the conduction and valence band of the silicon substrate (e.g., work function of about 4.7 electron-volts). One key drawback of mid-bandgap metals, however, is their inability to achieve the small threshold voltage (V_T) necessary for future CMOS technology scaling, without degrading short channel effects.

A complementary metal gate approach with two work functions, optimized for both NMOS and PMOS devices, respectively, thus far has yet to be integrated into a workable process. The simple method to deposit complementary metals, one after the other, would damage the thin gate dielectric during patterning of at least one of the electrodes making the transistor unusable.

What is needed is the incorporation of complementary metal gate electrode technology into a workable process that is scalable for future CMOS technologies.

SUMMARY OF THE INVENTION

A device is disclosed. The device includes a first transistor having a first metal gate electrode overlying a first gate dielectric on a first area of a semiconductor substrate. The first gate electrode has a work function corresponding to the work function of one of P-type silicon and N-type silicon. The device also includes a second transistor complementary to the first transistor. The second transistor has a second metal gate electrode over a second gate dielectric on a second area of the semiconductor substrate. The second metal gate electrode has a work function corresponding to the work function of the other one of P-type silicon and N-type silicon.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic side view illustration of a portion of a semiconductor substrate after the processing step of forming shallow trench isolation structures and well regions in the substrate and a gate dielectric over the surface of a substrate in accordance with a first embodiment of the invention.

Figure 2 shows the semiconductor substrate of **Figure 1** after the further processing step of depositing a metal layer over the gate dielectric in accordance with the first embodiment of the invention.

Figure 3 shows the semiconductor substrate of **Figure 1** after the further processing step of masking a portion of the metal layer over a region of the substrate in accordance with the first embodiment of the invention.

Figure 4 shows the semiconductor substrate of **Figure 1** during the processing step of exposing the unprotected portion of the metal layer to a chemically reactive ambient in accordance with the first embodiment of the invention.

Figure 5 shows the substrate of **Figure 1** after the further processing step of reacting the exposed metal layer with the chemically reactive ambient and removing the masking layer in accordance with the first embodiment of the invention.

Figure 6 shows the substrate of **Figure 1** after the further processing step of patterning complementary gate electrodes in adjacent cell regions in accordance with the first embodiment of the invention.

Figure 7 shows the substrate of **Figure 1** after the further processing step of patterning complementary transistors in adjacent cell regions in accordance with the first embodiment of the invention.

Figure 8 shows a schematic side view illustration of the semiconductor substrate of **Figure 1** after the processing steps of forming cell regions with desired dopants in the substrate and forming a gate dielectric, a first metal layer, and a second layer of metal or other material over the top surface of the substrate in accordance with a second embodiment of the invention.

Figure 9 shows the substrate of **Figure 7** after the further processing step of patterning the second layer over one active region of the first metal layer in accordance with the second embodiment of the invention.

Figure 10 shows the substrate of **Figure 7** after the further processing step of reacting the second layer with the first metal layer in accordance with the second embodiment of the invention.

Figure 11 shows the substrate of **Figure 7** after the processing step of forming complementary transistor devices in

adjacent cell regions in accordance with the second embodiment of the invention.

Figure 12 shows a schematic side view illustration of a semiconductor substrate after the processing steps of forming complementary doped cell regions in the substrate and a gate dielectric material, a first metal layer, and a patterned mask over the substrate and shows the processing step of subjecting the unmasked portion of the metal layer to ion implantation in accordance with a third embodiment of the invention.

Figure 13 shows the substrate of **Figure 12** after the processing step of ion implantation and removal of the mask in accordance with the third embodiment of the invention.

Figure 14 shows the substrate of **Figure 12** after the processing step of patterning complementary transistor devices in adjacent cell regions in accordance with the third embodiment of the invention.

Detailed Description of the Invention

A circuit device employing metal gate electrodes tuned for a work function similar to the desired device type is disclosed. The invention is particularly useful for, but not limited to, the utilization of metal gate electrodes in CMOS technology tuned for optimum NMOS and PMOS device performance. The invention offers a workable process for providing integrated complementary metal gate electrode technology that is scalable for future CMOS technologies.

The invention describes metal gate electrodes or their compounds having Fermi levels close to either N-type or P-type doped silicon. It is to be appreciated that the suitable metal may exist at the desired Fermi level in its natural state or by chemical reaction, alloying, doping, etc. One aspect of the invention described herein is directed at workable methods of modifying metals for optimum NMOS and PMOS device performance.

Figures 1-7 illustrate an embodiment of a method of forming a CMOS structure utilizing the complementary gate electrode technology of the invention. **Figure 1** shows semiconductor substrate 100, such as a silicon substrate, or epitaxial layer 100 of a semiconductor substrate having active areas or cell regions defined by shallow trench isolation structures 110 formed in substrate or epitaxial layer 100. In this embodiment, shallow trench isolation structures 110 define active areas or cell regions for individual transistor devices.

Figure 1 also shows the formation of wells 105 and 115 in the individual active area or cell region defined by shallow trench isolation structures 110. For example, P-type well 105 is formed in one region of substrate 100 while N-type well 115 is formed in a second region of substrate 100. P-type well 105 is formed by diffusing a dopant, such as boron, into the substrate. N-type well 115 is formed by diffusing a dopant, such as arsenic, phosphorous, or antimony into substrate 100. The practices of forming shallow trench isolation structures 110 and wells 105 and 115 are known in the art and are therefore not presented herein.

Figure 1 still also shows substrate 100 after the further processing step of forming a gate dielectric over the surface of substrate 100. Gate dielectric layer 120 may be grown or deposited. An example of gate dielectric material that is typically grown by thermal techniques over substrate 100 is silicon dioxide (SiO_2). It is to be appreciated that, in addition to SiO_2, other gate dielectrics may be used to further optimize the CMOS transistor devices. For example, gate dielectric materials having a high dielectric constant may be utilized if desirous, for example, to increase the capacitance of the gate.

After gate dielectric layer 120 is formed, **Figure 2** shows the substrate of **Figure 1** after the further processing step of depositing metal layer 130 over the surface of substrate 100. In this embodiment, metal layer 130 is deposited to thickness a

of, for example, 500-2000 Å. In the embodiments that are described herein, the physical properties of at least a portion of metal layer 130 will be modified to adjust the work function for optimum NMOS and PMOS device performance. Thus, metal layer 130 will serve in its present state or in a modified state as a gate electrode. Accordingly, the thickness of metal layer 130 is scalable and should be chosen based primarily on integration issues related to device performance. Further, since in many of the embodiments that are described herein, the physical properties of metal layer 130 will be modified, care should be taken to avoid making metal layer 132 too thick so that, when desired, any modification or transformation of metal layer 130 is complete.

Figure 3 shows the substrate of **Figure 1** after the further processing step of patterning masking layer 135 over a portion of metal layer 130. In this embodiment, masking layer 135 is patterned over the active area or cell region represented by P-type well 105. Thus, the portion of metal layer 130 over active area or cell region denoted by N-type well 115 is exposed.

In one embodiment, mask layer 135 is an inactive hard mask material. Mask layer 135 material is inactive inasmuch as it will not participate in a chemical reaction with metal layer 130. Suitable inactive mask materials for masking layer 135 include, but are not limited to, SiO_2 and silicon nitride (Si_3N_4).

In one embodiment, metal layer 130 is tantalum (Ta). One analysis of the work function of tantalum identifies its Fermi level or work function as between 4.15 and 4.25 electron-volts. Thus, tantalum itself may act as a suitable gate electrode material for an N-type device. Accordingly, in this example, metal layer 130 is protected by hard mask 135 over active areas or cell regions denoted by P-type well 105, i.e., active areas or cell regions that may accommodate an N-type device. In this example, masking layer 135 is an inactive hard mask such as SiO_2 or Si_3N_4.

As shown in **Figure 4**, substrate 100 is then exposed to an ambient such as ammonia (NH_3) or nitrogen (N_2). The reactive ambient interacts with the exposed areas of metal layer 130 overlying N-type well 115. In the case of a tantalum metal layer, the interaction and reaction between tantalum and NH_3 or N_2 produces a metal layer of tantalum nitride (TaN) over N-type well region 115. A TaN metal layer has a reported work function of 5.41 electron volts, suitable for use as a P-type gate electrode.

In another embodiment, masking layer 135 may be made of an active material. In this manner, masking layer 135 may inhibit the reaction by a subsequent processing step (e.g., serve as a mask to a subsequent processing step) while itself reacting with metal layer 130 over the active areas or cell regions denoted by P-type well 105. A suitable active mask includes, but is not limited to, undoped polysilicon. Polysilicon may react with

metal layer 130 to form a silicide. In an example of an active mask of polysilicon, metal layer 130 is, for example, molybdenum (Mo). The exposed area of metal layer 130 is exposed to an NH_3 or N_2 ambient as shown in **Figure 4**. The unprotected molybdenum reacts with the ambient to form molybdenum nitride (MoN) that has a reported work function of 5.33 electron-volts (P-type). At the same time, through the addition of heat, such as for example, 850°C, polysilicon masking layer 135 reacts with the molybdenum over active areas or cell regions denoted by P-type well 105 to form molybdenum silicide. Molybdenum silicide has a reported work function of 4.25 electron-volts (N-type).

Figure 5 shows substrate 100 after the further processing step of removing inactive mask 135 from the area above metal layer 130 over the active area or cell region denoted by P-type well 105. Alternatively, **Figure 5** shows substrate 100 after the further processing step of reacting the exposed portion of metal layer 130 with reactive ambient 138 and the protected portion of metal layer 130 with active mask 135. Accordingly, in either embodiment, **Figure 5** shows a metal layer overlying substrate 100 having tuned or optimum work functions for the particular electrode device that will be used in the respective active area or cell region. For example, **Figure 5** shows a portion of metal layer 130, such as for example tantalum, overlying the active area or cell region denoted by P-type well 105. Metal layer 130, such as for example tantalum, has a work function corresponding to the work function of an N-type device, identifying the availability of a metal gate electrode with a

tuned work function for an NMOS device in connection with P-type well 105. Conversely, **Figure 5** shows metal layer 132 over an active area or cell region denoted by N-type well 115. Metal layer 132 was formed by the reaction of metal layer 130 with reactive ambient 138 as described above. Metal layer 132 is, for example, tantalum nitride (TaN) having a work function of 5.41 electron-volts. Thus, metal layer 132 is tuned or optimized for a gate electrode of a PMOS device associated with N-type well 115.

Figure 6 shows substrate 100 after the further processing step of patterning the individual metal layers 130 and 132 over their respective device regions. As shown in **Figure 6**, N-type metal layer 130 is formed into metal gate electrode 130 over the region of substrate 100 occupied by P-type well 105. P-type metal layer 132 is patterned into P-type gate electrode 132 over an area of substrate 100 occupied by N-type well 115. Metal layers 130 and 132 are patterned using conventional techniques such as a plasma etchant. In the case of tantalum and TaN, for example, a suitable etchant is a chlorine-based etch chemistry. Patterned in accordance with electrodes 130 and 132 is gate dielectric 120.

Figure 7 shows substrate 100 after the further processing step of forming diffusion or junction regions in substrate 100 in accordance with the characteristics of the desired device. With respect to the N-type device identified by N-type gate electrode 130 overlying P-well 105, N-type diffusion or junction

regions 133 are formed in P-well 105 in accordance with conventional techniques. For example, N-type diffusion or junction regions 133 may be formed adjacent gate electrode 130 and self-aligned to gate electrode 130 by implanting a suitable dopant such as, for example, arsenic, phosphorous, or antimony, into P-well 105. Similar processing steps may be used to form P-type regions 134, using a dopant, such as, for example, boron. Once diffusion or junctions regions 133 and 134 are formed, gate isolation spacers 152 of a suitable dielectric may be incorporated around gate electrode 130 and gate electrode 132 to insulate the individual electrodes of the transistor devices.

The process described above with respect to **Figures 1-7** illustrate the process of utilizing metal gate electrodes in CMOS technology tuned for optimum NMOS and PMOS performance. To make a CMOS structure, the NMOS and PMOS devices described above are coupled in an appropriate manner. **Figure 7** illustrates the coupling of NMOS device 141 and PMOS device 142 for an inverter.

Figures 8-11 illustrate a second process of forming complementary gate electrodes for optimum NMOS and PMOS device performance. In this process, as shown in **Figure 8**, semiconductor substrate or epitaxial layer 100 of a substrate has P-type well 105 and N-type well 115 formed in substrate or epitaxial layer 100 defining active area or cell region by shallow trench isolation structures 110. Overlying substrate 100 is gate dielectric 120 as described above and metal layer 130 deposited to a scalable thickness of, for example,

approximately 500-2000 Å. In one embodiment, metal layer 130 is chosen to have an appropriate work function for one of an NMOS gate electrode and a PMOS gate electrode (e.g., about 4.1 electrons-volts or 5.2 electron-volts, respectively). Alternatively, metal layer 130 may require subsequent modification to tune the material to an appropriate work function for an NMOS device. Deposited over metal layer 130 in **Figure 8** is second metal or other material layer 160.

Figure 9 shows the structure after the further processing step of patterning second metal or other material layer 160 over a portion of metal layer 130. In this case, second metal layer 160 is patterned over the active area or cell region denoted by N-type well 115. Metal layer 130 overlying P-type well 105 is left exposed.

Next, the structure is exposed to a heat treatment, such as for example, a high temperature (e.g., 900-1000°C) or laser anneal, to drive the reaction or combination of second metal or other material layer 160 and metal layer 130 to form a metal alloy or other compound. **Figure 10** shows substrate 100 after the further processing step of subjecting metal layer 130 to a heat treatment and forming a metal alloy or other metal compound over N-type well 115. The metal alloy or metal compound 165 is selected to have an appropriate work function for a PMOS device. Examples of suitable metal alloys or metal compounds formed in the manner described include, but are not limited to, molybdenum silicide.

Figure 11 shows substrate 100 after the further processing step of patterning metal layers 130 and 165 into metal gate electrodes and forming NMOS transistor device 161 and PMOS transistor device 162 by a process such as described above with reference to **Figures 6** and **7**. NMOS transistor device 161 includes doped diffusion or junction regions 170 and PMOS transistor device 162 includes doped diffusion or junction regions 175. Finally, as an example, **Figure 11** illustrates the coupling of NMOS device 161 and PMOS device 162 for an inverter.

In the process described, second metal layer 160 is described as a metal material that interacts or reacts with metal layer 130 and forms an alloy of metal compound with a desired work function. It is to be appreciated that second metal layer 130 could also be polysilicon. In this manner, the reaction between metal layer 130 and polysilicon layer 160 may be a silicide reaction to form a metal silicide having an appropriate work function. It is also to be appreciated that the process may be reversed. In other words, metal layer 130 could be patterned as a polysilicon layer with second metal layer 160 being an appropriate metal to form a metal silicide in accordance with the invention. One approach where the latter process might be preferred is the situation, for example, where only the NMOS transistor devices of the CMOS circuit utilize metal gate electrode with an optimized work function (i.e., Fermi level of approximately 4.5 electron-volts). Since, in many CMOS circuits, the performance of the NMOS device is more critical than the performance of the PMOS device, the process

described herein offers a workable method of optimizing NMOS device performance while leaving PMOS device performance relatively unchanged. Alternatively, two different metals can be deposited and patterned on the polysilicon layer to form two complementary silicides for the NMOS device and the PMOS device, respectively.

Figures 12-14 shows a third process of tuning the metal gate electrode of a CMOS circuit to optimum device performance by a process generally described as ion mixing. **Figure 12** again shows substrate 100 having P-type well 105 and N-type well 115 formed in substrate 100 or as part of active areas or cell regions defined by shallow trench isolation structures 110. Overlying substrate 100 is gate dielectric layer 120. Overlying gate dielectric 120 is metal layer 130.

Figure 12 shows substrate 100 after the further processing step of adding masking layer 180, such as for example, a hard inactive mask of SiO_2 or Si_3N_4 over that portion of substrate 100 denoted by P-type well 105. In one embodiment, metal layer 130 is chosen, for example, to have a work function corresponding to that of N-type doped silicon (i.e., about 4.1 electron-volts). In this manner, metal layer 130 may be patterned over the active area or cell region associated with P-type well 105 to form an NMOS device with a gate electrode tuned for optimum device performance. Alternatively, masking layer 180 may be an active mask, such as for example, a polysilicon, that may react with metal layer 130 in the presence of heat to

form a metal silicide having a work function corresponding to the work function of N-type doped silicon.

Figure 12 shows the further processing step of subjecting the exposed portion of metal layer 130 to an ion implantation 185. The ion implantation step seeks to implant a dosage of ions into the exposed portion of metal layer 130 to modify the work function of metal layer 130. In the embodiment presented, for example, ions are implanted and the implanted metal is annealed (by heat or laser) to modify the work function of metal layer 130 material into a P-type work function metal layer material. **Figure 13** shows substrate 100 after the further processing step of implanting a sufficient dosage of ion to modify the work function of metal layer 130 over active area or cell region denoted by N-type well 115. The modified metal is represented by P-type metal layer 190.

Figure 14 shows substrate 100 after the further processing step of forming NMOS device 191 and PMOS device 192 utilizing tuned metal gate electrode 130 and 190 over an active area or cell region denoted by P-type well 105 and N-type well 115, respectively. NMOS device 191 includes metal gate electrode 130 having a work function corresponding approximately to the work function of the N-type doped silicon, with N-type doped diffusion or junction region 495. Similarly, PMOS device 192 has metal gate electrode 190 having a work function corresponding approximately to the work function of P-type doped silicon with P-typed doped silicon diffusion or junction region

200 formed in substrate. Finally, **Figure 14**, as an example, illustrates the coupling of NMOS transistor device 191 and PMOS transistor device 192 for an inverter.

The above discussion presented various ways of turning metal gate electrode for optimum NMOS and PMOS device performance. The invention is particularly useful for, but are not limited to, the utilization of metal gate electrode in CMOS technology. The above discussion assumed that the gate electrode patterning is done after the modification of the metal layer. It is to be appreciated that the same modification of metal material may be accomplished by patterning the gate electrode first and modifying the gate electrode properties afterwards. Whichever sequence is better depends on how the process is integrated into the entire fabrication process.

In the preceding detailed description, the invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A circuit device comprising:

a first transistor including a first metal gate electrode overlying a over a first gate dielectric on a first area of a semiconductor substrate and having a work function corresponding to the work function of one of P-type silicon and N-type silicon; and

a second transistor complementary to the first transistor including a second metal gate electrode over a second gate dielectric on a second area of a semiconductor substrate and having a work function corresponding to the work function of the other one of P-type silicon and N-type silicon.

2. The integrated circuit device of claim 1, wherein the first metal gate electrode is one of a pure metal, a doped metal, and a metal alloy.

3. A method of forming a circuit device, comprising:

forming a gate dielectric overlying a region of a substrate;

depositing a metal layer over the gate dielectric; and

modifying the Fermi level of the metal layer.

4. The method of claim 3, further comprising the step of patterning the metal layer into a gate electrode.

5. The method of claim 3, wherein the step of modifying the Fermi level of the metal layer includes chemically reacting the metal layer with a compound.

6. The method of claim 5, wherein the region of the substrate includes a first region and a second region, and prior to the step of modifying the first metal layer, the method further comprises the step of:

masking the metal layer over the second region.

7. The method of claim 6, wherein the masking step includes masking with an inert compound.

8. The method of claim 6, wherein the masking step includes masking with a masking compound that reacts with the metal layer over the second region to modify the Fermi level of the reaction product.

9. The method of claim 8, wherein the masking compound is polysilicon.

10. The method of claim 3, wherein the step of modifying the Fermi level of the metal layer includes alloying the metal layer with one of a second metal layer and a silicon.

11. The method of claim 10, wherein the region of the substrate includes a first region and a second region, and the step of modifying the metal layer comprises modifying one of the first region and the second region.

12. The method of claim 11, wherein the step of alloying the metal layer includes alloying with a polysilicon.

13. The method of claim 3, wherein the step of modifying the Fermi level of the metal layer includes implanting an ion into the metal layer.

14. The method of claim 13, wherein the region of the substrate includes a first region and a second region, and the step of modifying the metal layer comprises modifying one of the first region and the second region.

15. The method of claim 14, wherein after the step of modifying the metal layer of one of the first region and the second region, the method comprises the step of modifying the other of the first region and the second region.

ABSTRACT OF THE DISCLOSURE

A circuit device that includes a first transistor having a first metal gate electrode overlying a first gate dielectric on a first area of a semiconductor substrate. The first gate electrode has a work function corresponding to the work function of one of P-type silicon and N-type silicon. The circuit device also includes a second transistor coupled to the first transistor. The second transistor has a second metal gate electrode over a second gate dielectric on a second area of the semiconductor substrate. The second gate metal gate electrode has a work function corresponding to the work function of the other one of P-type silicon and N-type silicon.

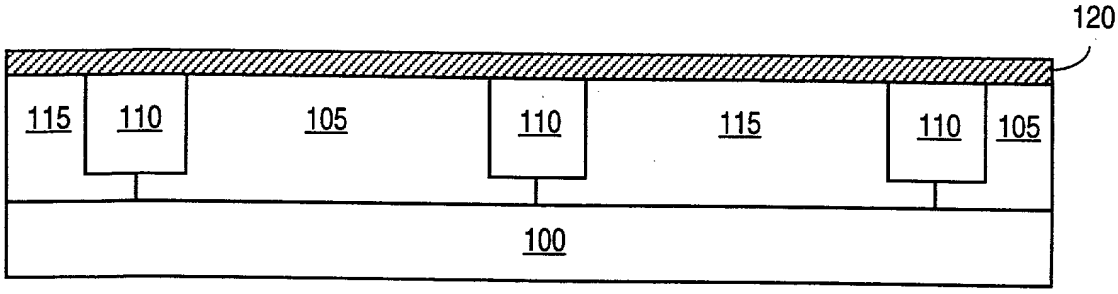
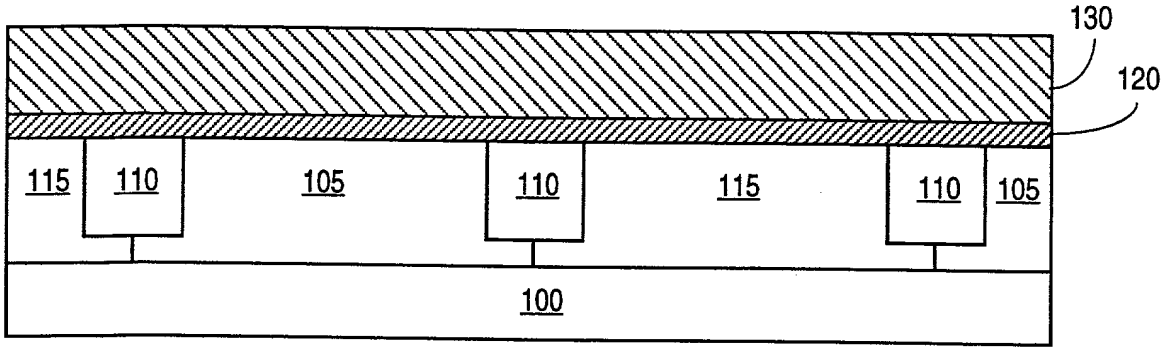


Fig. 1



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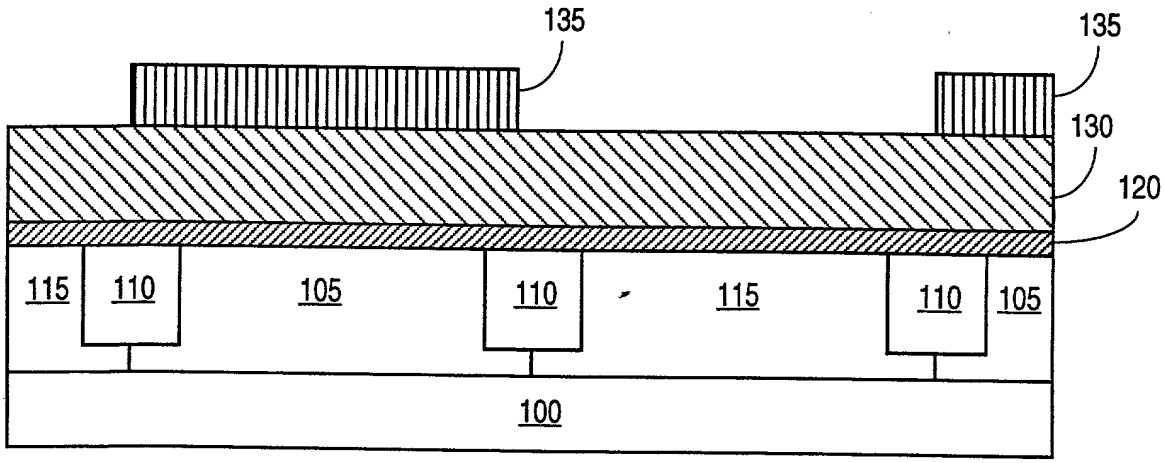

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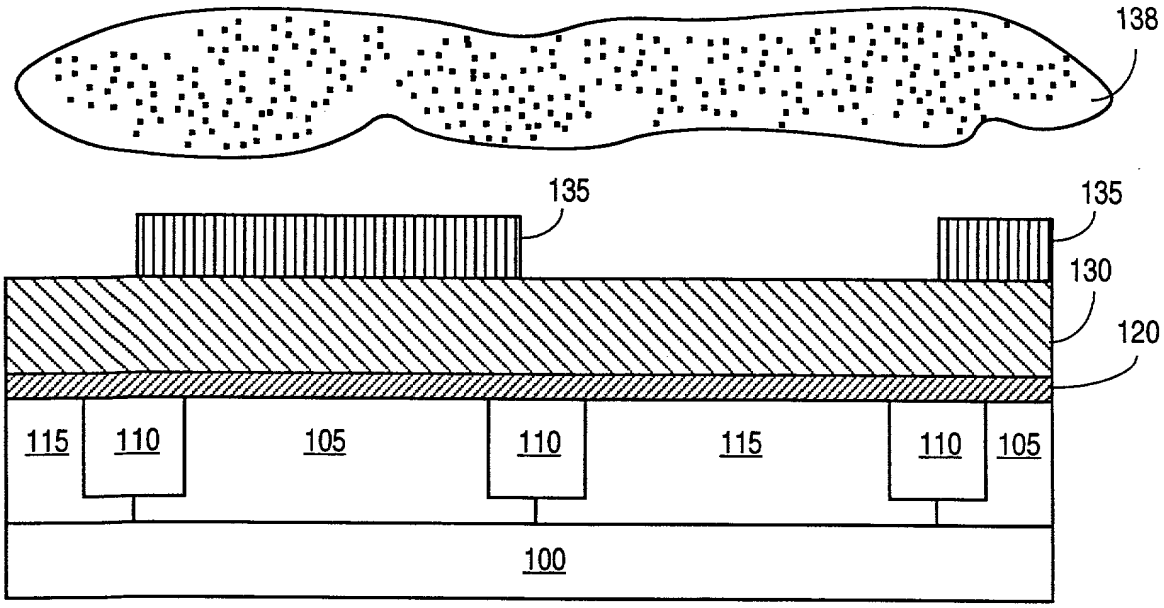

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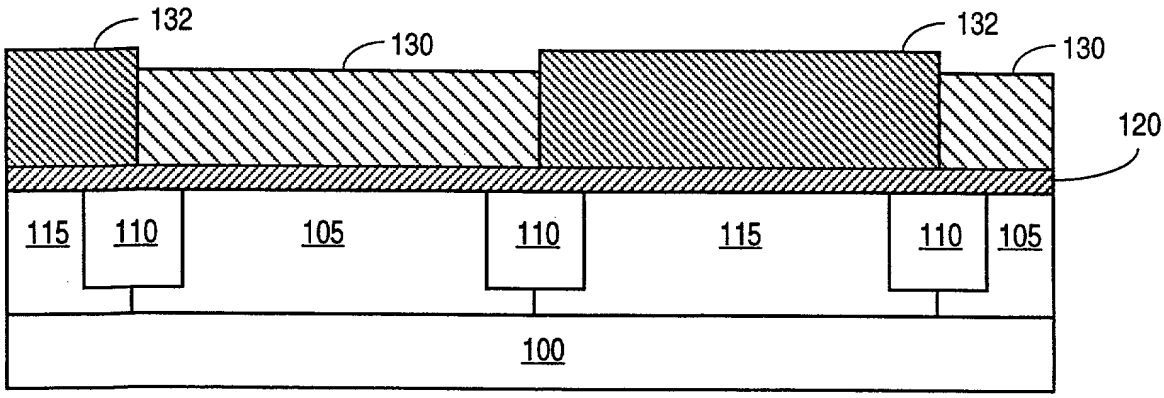

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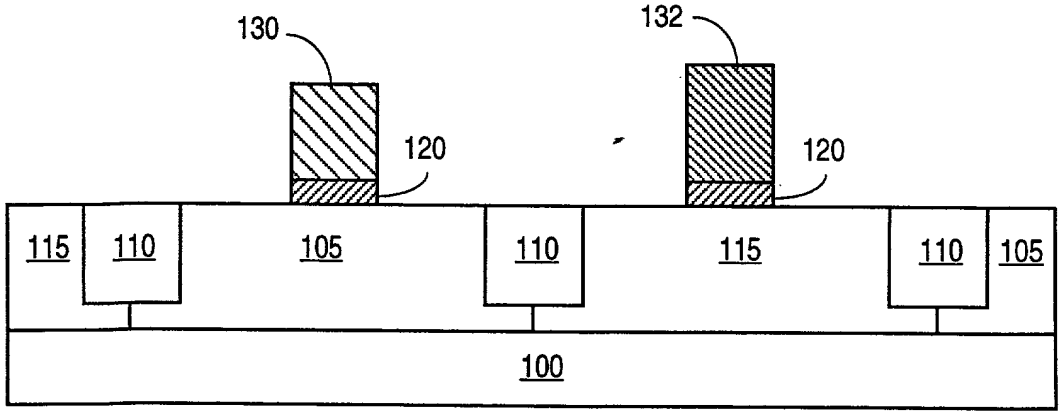

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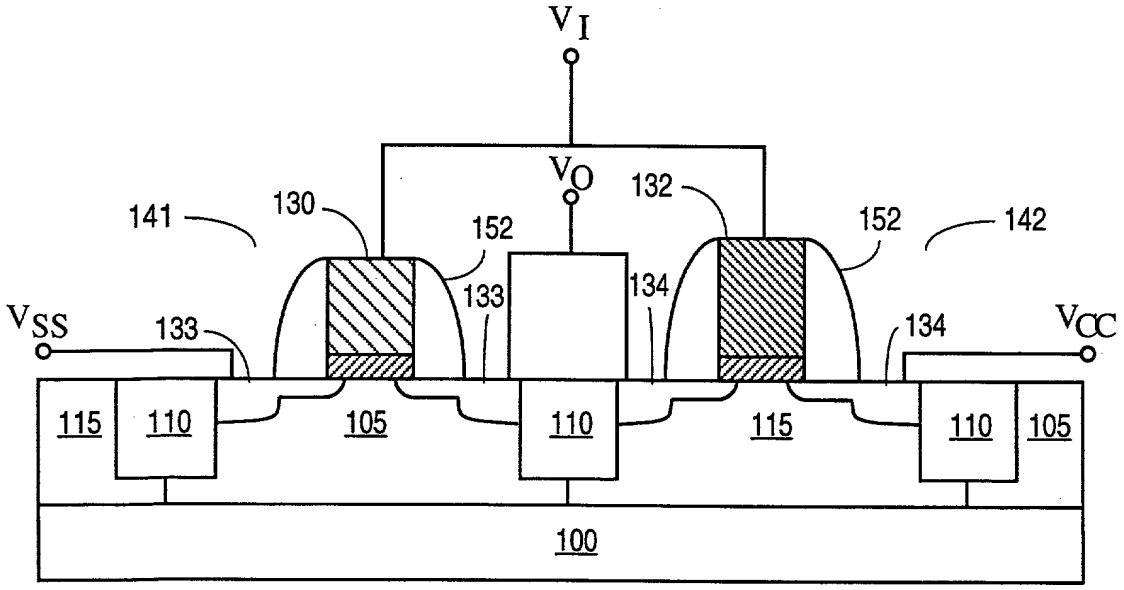

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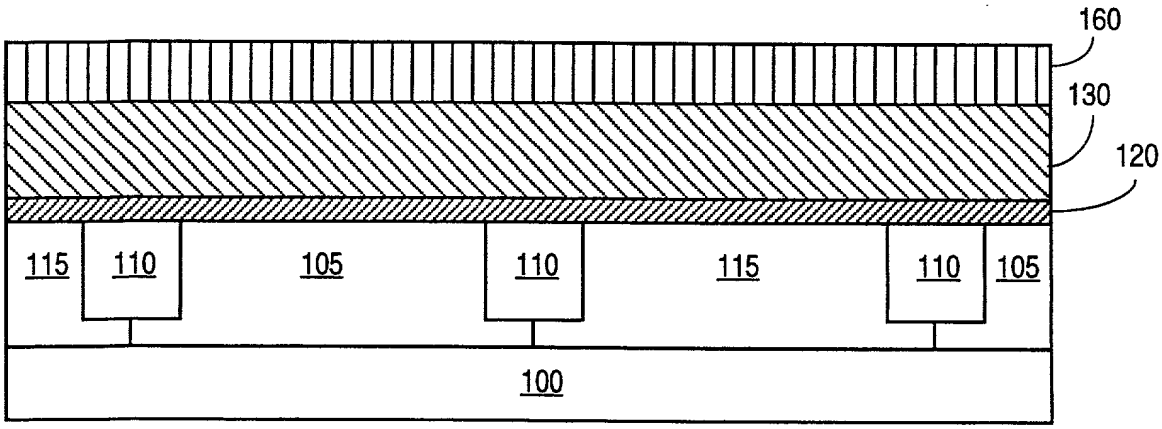
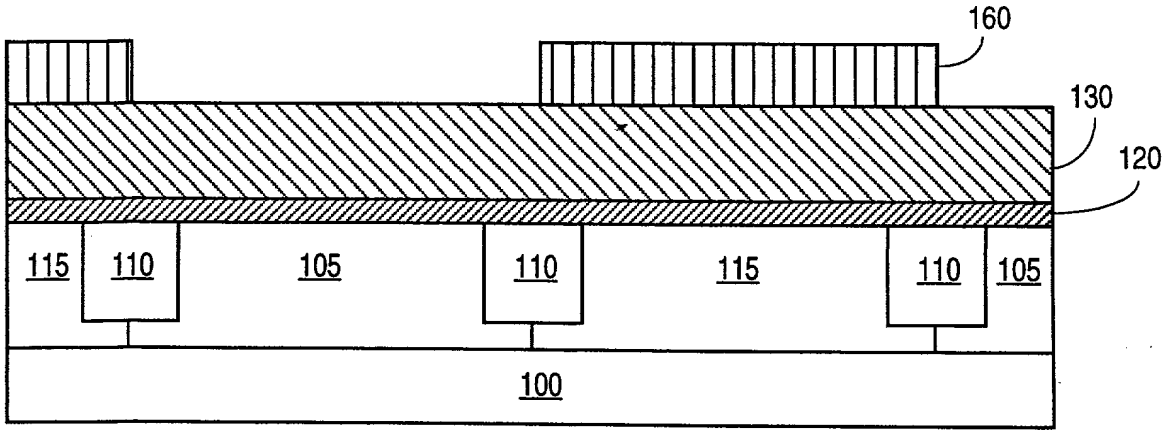


Fig. 8



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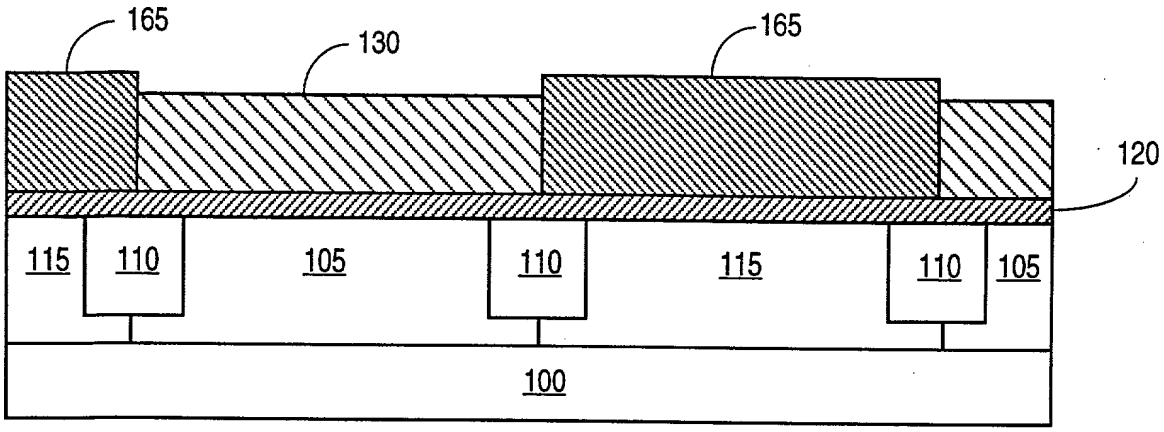


Fig. 10

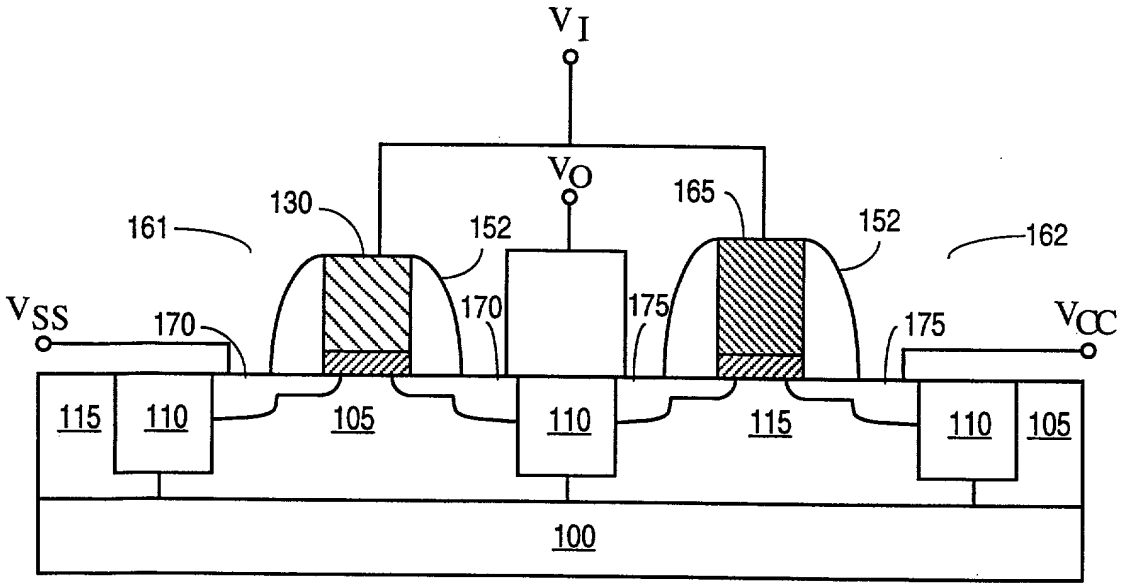


Fig. 11

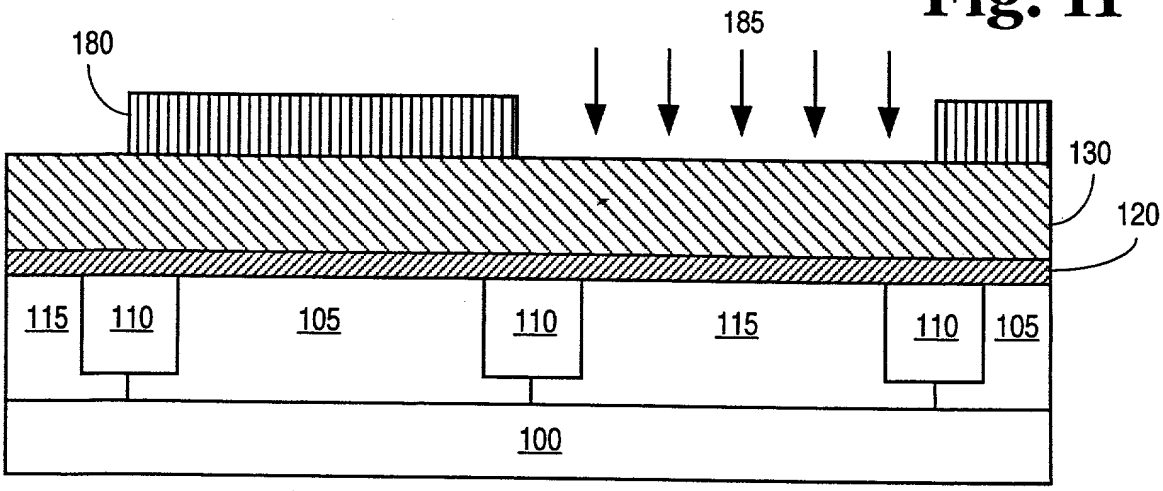
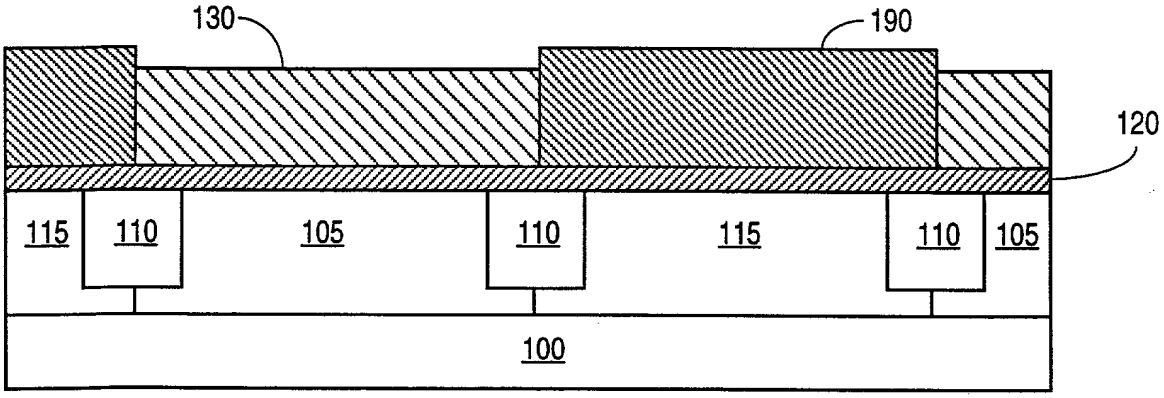


Fig. 12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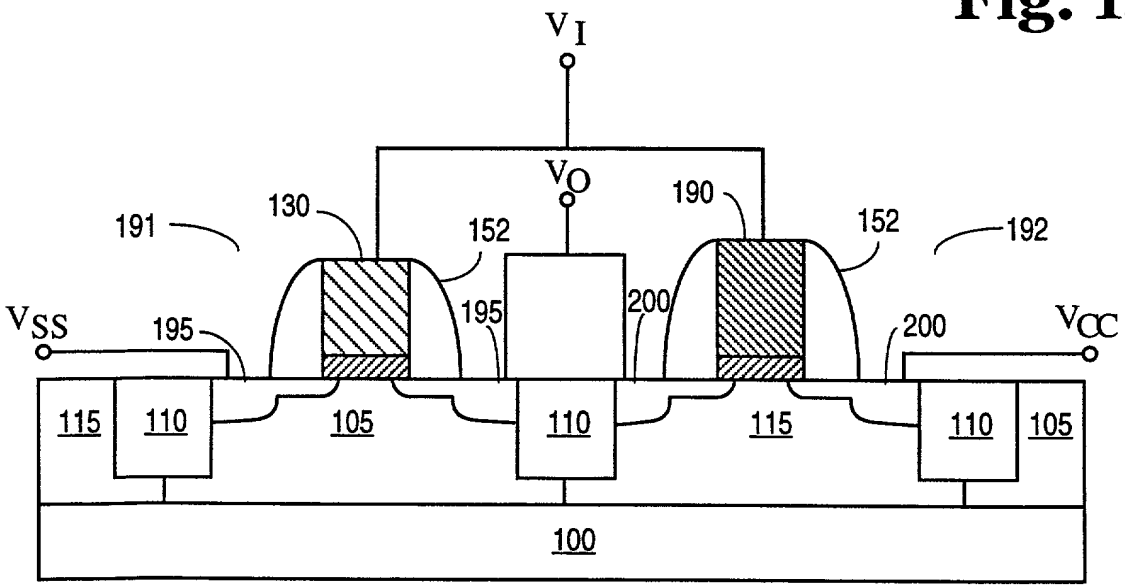
110
105
110
115
110
105
100

Fig. 13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V_O
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152
190
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V_{SS}
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195
200
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V_{CC}
115
110
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110
115
110
105
100

Fig. 14

Attorney's Docket No.: 042390.P5771

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Complementary Metal Gate Electrode Technology

the specification of which

[X] is attached hereto.

[ ] was filed on June 30, 1998 as
United States Application Number 09/107,604
or PCT International Application Number _____
and was amended on _____ .
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, a firm including: Farzad E. Amini, Reg. No. 42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, P41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. P42,442; William Donald Davis, Reg. No. 38,428; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Tarek N. Fahmi, Reg. No. P41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., P42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, P41,839; Willmore F. Holbrow III, Reg No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Tim L. Kitchen, Reg. No. P41,900; Michael J. Mallie, Reg. No. 36,591; Paul A. Mendonsa P42,879; Darren J. Milliken, P42,004; Thinh V. Nguyen, Reg. No. P42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch P43,021; Babak Redjaian, Reg. No. P42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. 43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; Geoffrey T. Staniford, P43,151; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, P43,237; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Amy M. Armstrong, Reg. No. P42,265; Robert Andrew Diehl, Reg. No. P40,992; and Edwin A. Sloane, Reg. No. 34,728; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Sean Fitzgerald, Reg. No. 32,027; James E. Jacobson, Jr., Reg. No. 31,626; Seth Z. Kalson, Reg. No. 40,670; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Howard A. Skaist, Reg. No. 36,008; and Raymond J. Werner, Reg. No. 34,752; my patent attorneys, of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to William Thomas Babbitt, Reg. No. 39,591, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP,
(Name of Attorney or Agent)
12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to William Thomas Babbitt, Reg. No. 39,591, (310) 207-3800.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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INTEL CORPORATION

Docket No. 042390.P5771

Full Name of Second/Joint Inventor (given name, family name) **Gang Bai**

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Full Name of Third/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City , State) *(Country)*

P. O. Address _____

_____

Full Name of Fourth/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City , State) *(Country)*

P. O. Address _____

_____

Full Name of Fifth/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City , State) *(Country)*

P. O. Address _____

_____